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Group 2700

37 CFR 1.501
INFORMATION DISCLOSURE STATEMENT
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Docket No. P99,0886	Serial No. 09/308,478
Applicants Utz Wever, et al.	
Filing Date May 17, 1999	Group Art Unit

U.S. PATENT DOCUMENTS

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OTHER PRIOR ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	AT	I. Hofer, et al., SPICE Analyseprogramm fur elektronische Schaltungen, Springer, Berlin (1985), pp. 7-22
DWS	AU	U. Kleis, et al., <i>Domain Decomposition Methods for Circuit Simulation</i> , Proceedings of the 8 th Workshop on Parallel and Distributed Simulation, PADS, Edinburgh, UK (July, 1994), pp. 183-86
DWS	AV	U. Wever, et al. <i>Parallel Transient Analysis for Circuit Simulation</i> , Proceedings of the 29 th Annual Hawaii International Conference on System Sciences (1996), pp. 442-47
DWS	AW	B. Riess, et al., <i>Partitioning Very Large Circuits Using Analytical Placement Techniques</i> , Proceedings of the 31 st ACM/IEEE Design Automation Conference (1994), pp. 646-51
DWS	AX	P. Johannes, <i>Partitioning of VLSI Circuits and Systems</i> , 33 rd Design and Automation Conference, Las Vegas (June 3-7, 1996), pp. 83-87

Examiner: Doug Sargent

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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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Docket No.
P99,0887

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09/308,304

Applicants
Utz Wever, et al.

Filing Date
May 17, 1999

Group Art Unit

U.S. PATENT DOCUMENTS

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	BP							
	BQ							
	BR							
	BS							

OTHER PRIOR ART (Including Author, Title, Date, Pertinent Pages, Etc.)

DWS	BT	J. Cong, et al., <i>A Parallel Bottom-up Clustering Algorithm with Applications to Circuit Partitioning in VLSI Design</i> , In: 30 th Design Automation Conference, June 14-18, 1993, pp. 755-760
DWS	BU	J. Li, et al., <i>New Spectral Linear Placement and Clustering Approach</i> , 33 ^d Design Automation Conference, Las Vegas (June 3-7, 1996), pp. 88-93
DWS	BV	T. Kage, et al., <i>A Circuit Partitioning Approach for Parallel Circuit Simulation</i> , IEICE Trans Fundamentals, Vol. E77-A, No. 31 (1993), pp. 461-65
DWS	BW	G. Hung, et al., <i>Improving the Performance of Parallel Relaxation-Based Circuit Simulators</i> , IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, New York (November 12, 1993), No. 11, pp. 1762-74
	BX	

Examiner

Doug Seige

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